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PAPER

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COOK, ALEX, MCFARRON, MANZO,			EXAMINER SCHECHTER, ANDREW M	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Application No. Applicant(s) 09/848,642 YAMAZAKI ET AL. Office Action Summary Examiner Art Unit ANDREW SCHECHTER 2871 -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS. WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). Status 1) Responsive to communication(s) filed on 29 May 2009. 2a) This action is FINAL. 2b) This action is non-final. 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) Claim(s) 21-24.76.77 and 85-102 is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) Claim(s) 21-24.76.77.85-90.93.94.97 and 98 is/are allowed. 6) Claim(s) 91.92.95.96 and 99-102 is/are rejected. 7) Claim(s) _____ is/are objected to. 8) Claim(s) _____ are subject to restriction and/or election requirement. Application Papers 9) The specification is objected to by the Examiner. 10) ☐ The drawing(s) filed on 05 March 2004 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abevance. See 37 CFR 1.85(a). Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner, Note the attached Office Action or form PTO-152. Priority under 35 U.S.C. § 119 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) □ Some * c) □ None of: Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. Attachment(s) 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) Paper No(s)/Mail Date. Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) Notice of Informal Patent Application

Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date ______.

6) Other:

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DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 29 May 2009 has been entered.

Response to Arguments

Applicant's arguments filed 29 May 2009 have been fully considered but they are
not persuasive. Applicant's arguments have been considered but are moot in view of
the new ground(s) of rejection.

The applicant details [pp. 12-13] the element matching between the limitations of claims 91 and 92 and their invention as shown in Fig. 16 and argues that the amended claims therefore are supported by the specification as filed. This is persuasive, so the previous rejections of claims 91 and 92 under 35 USC 112, 1st paragraph, are withdrawn. (To avoid possible confusion in the future, the examiner notes that the applicant refers to element 1006 as the "source wiring" in the specification but refers to element 1023 as the "source wiring" in the claims. The term is reasonable for either.)

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However, the additional limitations of claims 101 and 102, reciting a gate wiring on the second insulating film, electrically connected to the gate electrode, and a connection wiring electrically connecting the source wiring and the source region and formed on the second insulating film, are not shown in Fig. 16 and those claims are still not supported by the specification. These claims continue to be rejected below under 35 USC 112, 1st paragraph.

The scope of claims 91 and 92 have been broadened by the amendments to the claims; the following prior art rejections are therefore appropriate.

Claim Rejections - 35 USC § 112

- 3. The following is a quotation of the first paragraph of 35 U.S.C. 112:
 - The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
- 4. Claims 101 and 102 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The additional limitations of claims 101 and 102, reciting a gate wiring on the second insulating film, electrically connected to the gate electrode, and a connection wiring electrically connecting the source wiring and the source region and formed on the second insulating film, are not shown in Fig. 16 and are not supported by the

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specification when considered in combination with the limitations of the independent claims. For instance, Fig. 15 does not disclose the limitations of claims 91 and 92 that there are source and drain regions formed over the semiconductor layer and a second insulating film over the semiconductor layer, the source and drain regions and the second wiring, which is in contact with the channel formation region. The examiner does not see any specific support for the inventions of claims 101 and 102; the specification therefore does not reasonably convey that the applicant had possession of the claimed invention at the time of filing, so claims 101 and 102 are rejected.

Claim Rejections - 35 USC § 103

- The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 91, 92, 95, 96, 99, and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Yokomizu*, Japanese Patent Document No. 10-073813, in view of *Kanemoto et al.*, U.S. Patent No. 5,493,429, and *Yoneya et al.*, U.S. Patent No. 6,300,926, and further in view of *Noguchi*, U.S. Patent No. 5,289,016.

Yokomizu discloses [see Figs. 1 and 2, for instance] an electro-optical device comprising a first substrate [10], a thin film transistor [paragraph 0017] formed over the first substrate, a pixel electrode [13] comprising a first transparent conductive film [paragraph 0018], and electrically connected to the TFT, a second substrate [20]

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opposed to the first substrate, at least a first colored layer [21B] and a second colored layer [21R] formed on the second substrate wherein the first and second colored layers partly overlap each other to form a light shielding portion [21BM]; an organic resin film [22, paragraph 0021] covering said first and second colored layers and said light shielding portion, an opposing electrode [23] comprising a second transparent conductive film [paragraph 0021], and a liquid crystal [30] interposed between the pixel electrode and the opposing electrode, wherein the organic resin film is interposed between the liquid crystal and the first and second colored layers, and wherein the opposing electrode is interposed between the liquid crystal and the organic resin film.

Yokomizu does not disclose that the organic resin film has a thickness of 1 μ m or more; the reference appears to be silent on the thickness of the organic resin film. Kanemoto discloses [see Fig. 1] analogous overlapping color filters, and discloses that the thickness increase where they overlap is 1-2 μ m [col. 3, lines 34-36]. Yoneya teaches [col. 17, line 65 – col. 18, line 5] that a function of the organic resin film (overcoat layer) is "to flatten a difference in level due to the color filter and the light-shielding film". It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to make the thickness of the organic resin film large enough to flatten (or at least moderate) a 1-2 μ m bump. Doing so requires a thickness of about 1 μ m or more, which overlaps the recited range of 1 μ m or more; in such cases a prima facile case of obviousness exist [see MPEP 2144.05].

Yokomizu also does not necessarily disclose the TFT comprising a gate electrode; a first insulating film formed on said gate electrode; a semiconductor layer

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formed over said first insulating film, and having a channel formation region; a source region and a drain region formed over the semiconductor layer; a source wiring formed over said first substrate, the source wiring electrically connected to said source region through a second wiring; a second insulating film over said semiconductor layer, the source region, the drain region and the second wiring, wherein the second insulating film is in contact with the channel formation region; with the pixel electrode electrically connected to the drain region of the TFT.

Noguchi discloses [see Fig. 2, for instance] a TFT for an analogous LCD, wherein the TFT comprises a gate electrode [2]; a first insulating film [3] formed on said gate electrode; a semiconductor layer [4] formed over said first insulating film, and having a channel formation region [in the middle, in contact with layer 10]; a source region [5 to the left] and a drain region [5 to the right] formed over the semiconductor layer; a source wiring [8 to the left] formed over said first substrate, the source wiring electrically connected to said source region through a second wiring [7 to the left]; a second insulating film [10] over said semiconductor layer, the source region, the drain region and the second wiring; wherein the second insulating film is in contact with the channel formation region [see Fig. 2]; and with a pixel electrode [6] electrically connected to the drain region of the TFT. It would have been obvious to one of ordinary skill in the art at the time of the invention to use such a TFT in the above device, motivated by Noguchi's teaching that this suppresses an increase in the OFF current and reduces change in the ON current threshold voltage, thus improving the stability of

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the transistor characteristics with respect to other TFT designs. Claim 91 is therefore unpatentable.

Regarding the additional limitation of claim 92, that there is a third colored layer, Yokomizu discloses a third colored layer [21G]. (Regarding the previous limitation that all three colored layers are in the overlap stack, Yokomizu also discloses that all three color filters can be stacked to form 21BM [paragraph 0020, for instance]). Claim 92 is therefore also unpatentable.

A step (albeit tapered) exists at a portion where the colored layers overlap, so claims 95 and 96 are also unpatentable. The organic resin film is a leveling film, as discussed above with reference to *Yoneya*, so claims 99 and 100 are also unpatentable.

Allowable Subject Matter

- 7. Claims 21-24, 76, 77, 85-90, 93, 94, 97, and 98 are allowed.
- 8. The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not disclose the electro-optical device of claim 21, in particular the limitations reciting the following electrode structure: a gate electrode and source wiring, first insulating film formed on them, semiconductor layer formed over the first insulating film, second insulating film covering the semiconductor layer, and gate wiring (connected to gate electrode) and connection wiring (connecting source wiring to semiconductor layer) formed on the second insulating film. Claim 21 is therefore allowed, as are its dependent claims 22-24, 88-90, 93, and 97.

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The prior art does not disclose the electro-optical device of claim 76, in particular the limitations reciting the same electrode structure discussed above with respect to claim 21. Claim 76 is therefore allowed, as are its dependent claims 77, 85-87, 94, and 98.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/Andrew Schechter/ Primary Examiner, Art Unit 2871 Technology Center 2800 3 June 2009